## Feature

- High Precision GaAs process
- High performance, shielded
- GaAs substrate, 50Ω CPW output
- Au wire bonding, for MCM applications

## Environmental Specifications

| | |
|---|---|
| Operating Temperature | -55℃~+85℃ |
| Storage Temperature | -65℃~+150℃ |
| Max. Input Power | 30dBm |

## Electrical Specifications($T_A$=+25℃)

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Center Freq. ($f_0$) | - | 5.5 | - | GHz |
| Pass band | 5.25 | - | 5.75 | GHz |
| Insertion Loss @ $f_0$ | - | - | 3.0 | dB |
| Ripple in Pass band | - | - | 1.0 | dB |
| Return Loss | 12 | - | - | dB |
| Out of band Attenuation | ≥30@4.8GHz | | | dB |
| | ≥30@6.3GHz | | | dB |

S2P file name: PDBF-5R25_5R75-5D3.s2p

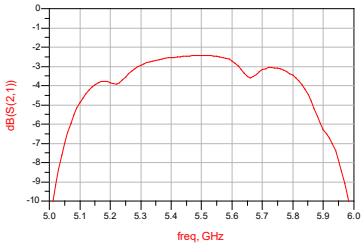
## Outline Drawing


Notes:

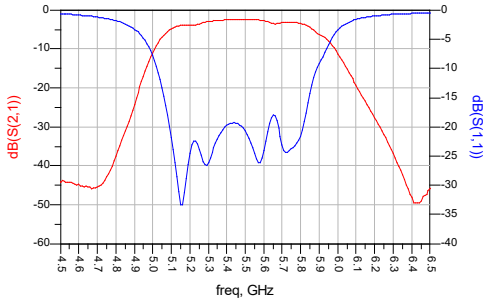
1. Dimensions are in millimeters. Tolerance: ±0.05mm
2. Die thickness is 0.15 mm
3. Typical bond pad is 0.1x0.1 $mm^2$.
4. The bottom of the device is gold plated, should be grounded.

## Typical Test Curves

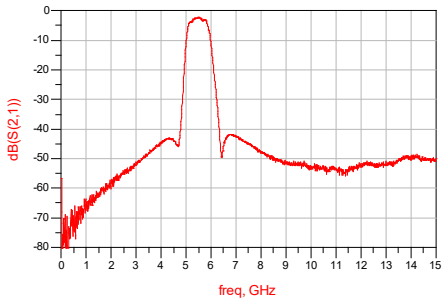
Insertion Loss VS Frequency ($T_A$=25℃)



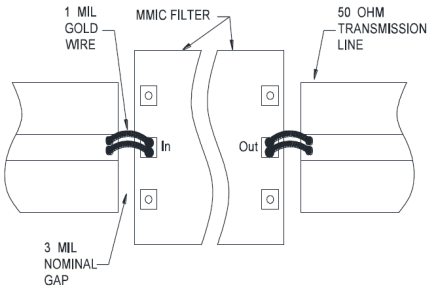

Insertion Loss & Return Loss VS Frequency ($T_A$=25℃)




Broadband Insertion Loss VS Frequency ($T_A$=25℃)




## Recommended Assembly Diagrams




## Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. (5.8×10-6/ ) with GaAs.
3. Recommend using Φ25um Au wire for bonding, whose length is around 400um.
4. Sinter by AuSn (80/20), which doesn't exceed 300℃ within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.