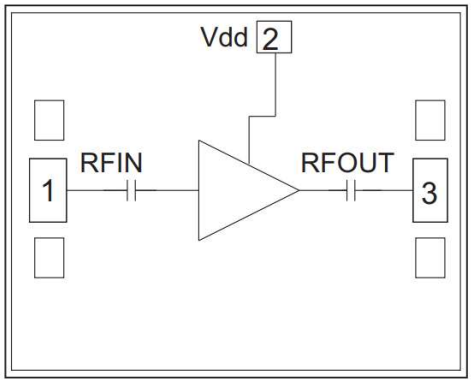
Performance

- Frequency: 4.0-8.0GHz
- Noise Figure: 1.0dB
- Gain: 22dB
- Gain Flatness: ±0.5dB
- P1dB output Power: 8dBm
- Psat: 10dBm
- Output IP3: 20dBm
- Single supply operation: +5V @ 50mA
- Input/Output Impedance: 50Ω
- Size: 1.7*1.1mm*0.07mm

Function Diagram



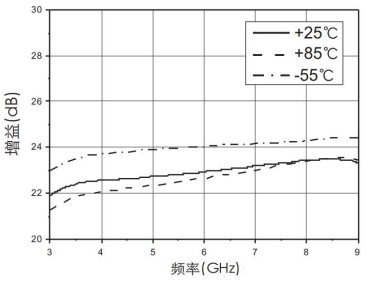
Electrical Specifications (T_A=+25℃, 50Ω system, Vdd=+5V, Idd=50mA, F: 4.0-8.0GHz)

Symbol	Parameter	Min	Typical	Max	Unit
G	Gain	-	22	-	dB
△G	Gain Flatness		±0.5		
NF	Noise Figure	-	1.0	-	dB
IRL	Input Return Loss	-	10	-	
ORL	Output Return Loss	-	10	-	
P1dB	1dB compression output power	-	8	-	
Psat	Saturated output power	-	10	-	
OIP3	IP3 output power	-	20	-	
Idd	Operating current	-	50	-	

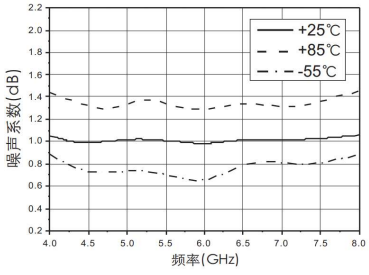
100% DC and RF wafter tested

Test Curves

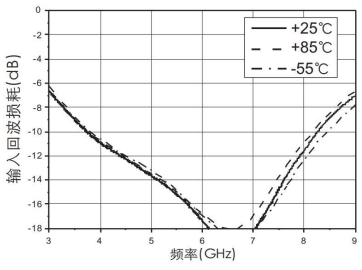
Small Signal Gain vs Freq vs Temp



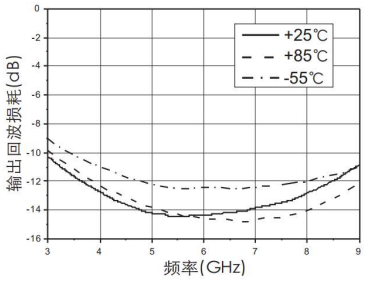
Noise Figure vs Freq vs Temp



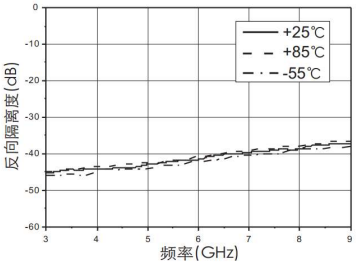
IRL vs Freq vs Temp



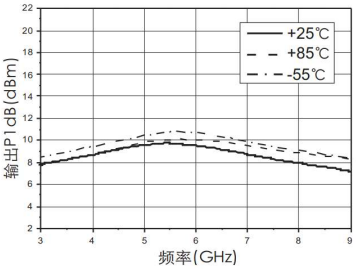
ORL vs Freq vs Temp



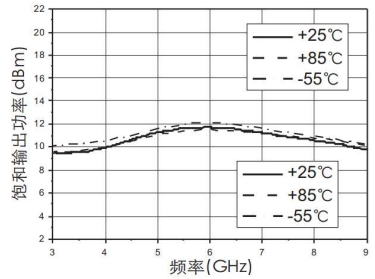
Reverse Isolation vs Freq vs Temp



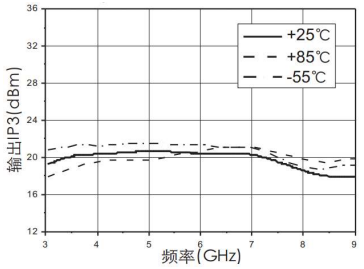
Output P1dB vs Freq vs Temp



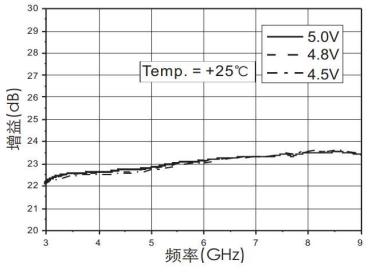
Psat vs Freq vs Temp



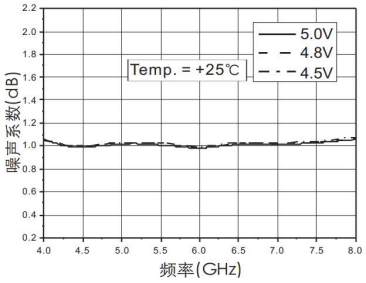
Output IP3 vs Freq vs Temp



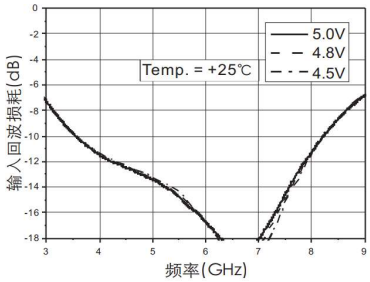
Small Signal Gain vs Freq vs Vdd



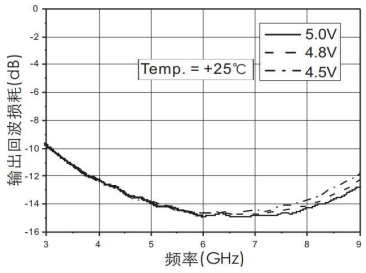
Noise Figure vs Freq vs Vdd



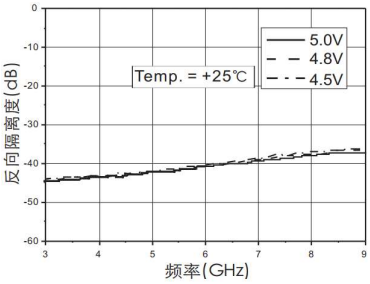
IRL vs Freq vs Vdd



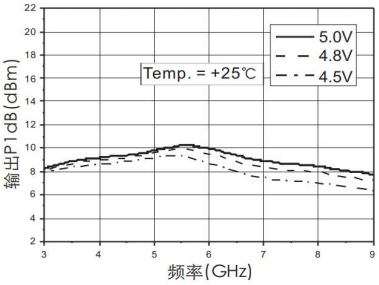
ORL vs Freq vs Vdd



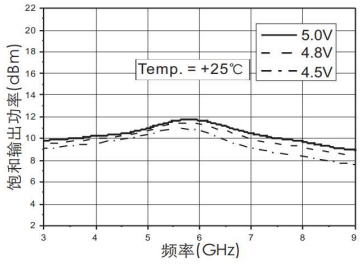
Reverse Isolation vs Freq vs Vdd



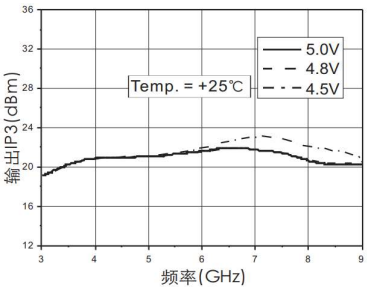
Output P1dB vs Freq vs Vdd



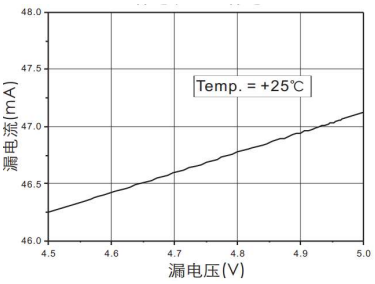
Psat vs Freq vs Vdd



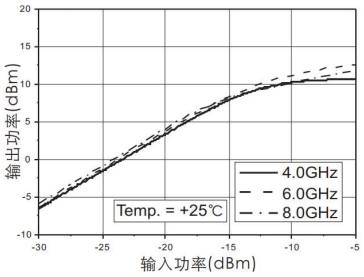
Output IP3 vs Freq vs Vdd



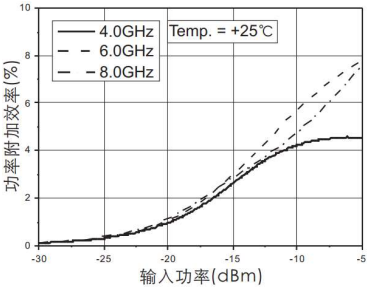
Idd vs Vdd



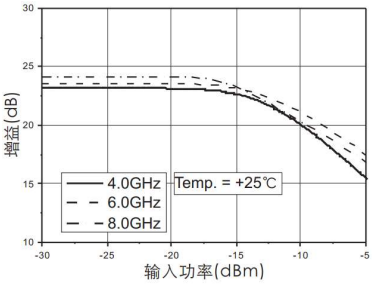
Output vs Input Power vs Freq



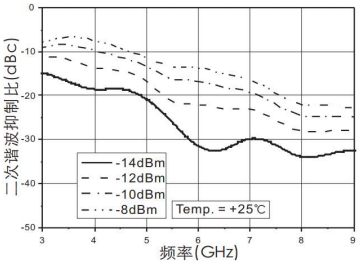
PAE vs Input Power vs Freq



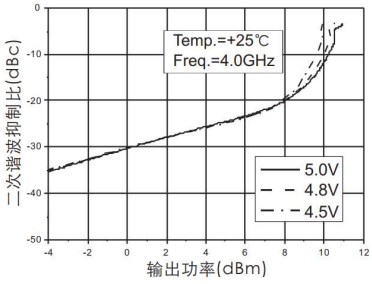
Gain vs Input Power vs Freq



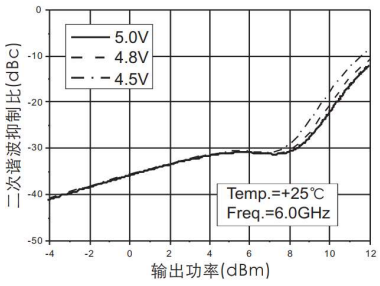
2nd Harmonic vs Freq vs Pin



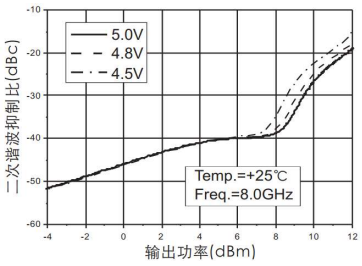
2nd Harmonic vs Pout vs Vdd



2nd Harmonic vs Pout vs Vdd



2nd Harmonic vs Pout vs Vdd

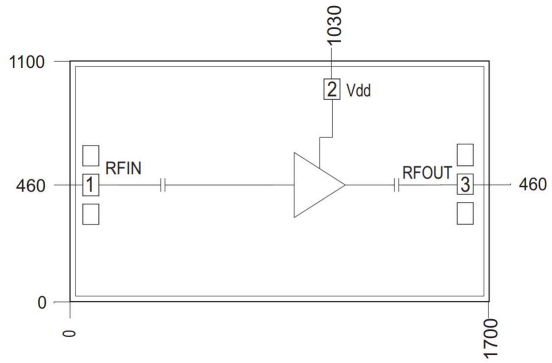


Absolute Max Ratings

Parameter	Value
Input Power PIN, 50Ω	+17dBm
Vdd	+6V
Rth	118.71℃/W
TCH	175℃
Junction Temperature	320℃
Storage Temperature	-55~+150℃
Operating Temperature	-55~+125℃

Exceeding any one or combination of these limits may cause permanent damage.

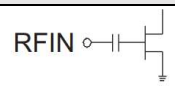
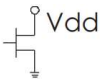
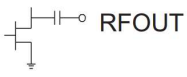
Outline Size



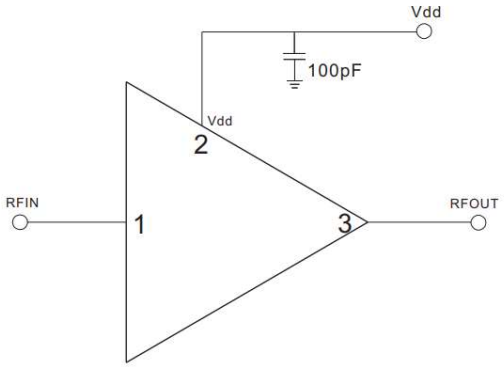
Note

1. Unit: μm
2. Bottom is gold plated
3. Bottom is grounded
4. Bonding pads are gold plated:
   1、3: 200*100μm，2、100*100μm
5. Don't bonding on through holes
6. Tolerance: ±50μm

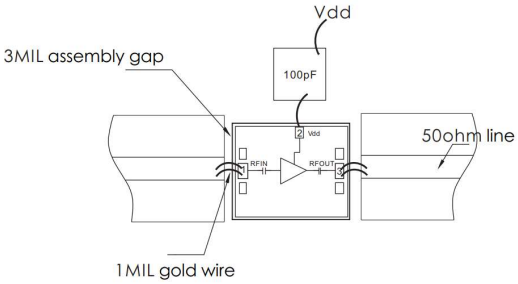
Bonding Pads Definition

Number	Symbol	Description	Equivalent circuit
1	RF in	RF input port, connect to 50Ω system, no block capacitor needed	
2	Vdd	Amplifier Drain Bias, external 100pF passby capacitor needed	
3	RF out	RF output port, connect to 50Ω system, no block capacitor needed	
Bottom	GND	Bottom has to be grounded	

Application Circuits



Assembly



Try to reduce the bonding line length by putting filter capacitor close to the pads.