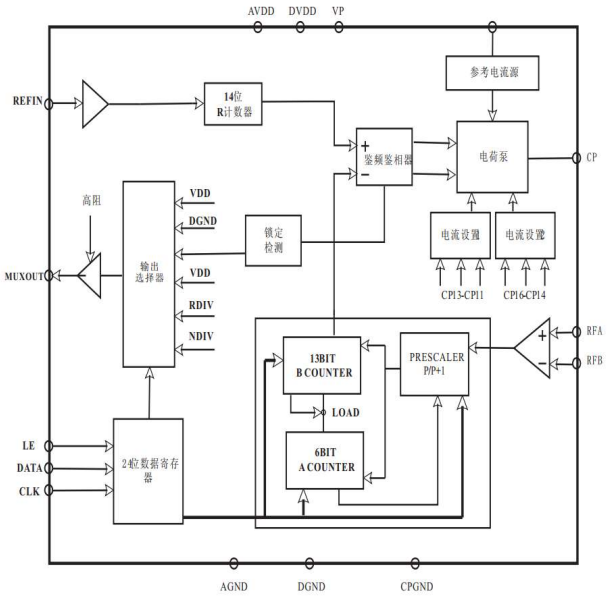
Performance

- Frequency: 0.8~6.5GHz
  (-10~10dBm)
- Reference Input: 20~350MHz
  (0.7V~VDD)
- Phase Frequency: 100MHz
- Noise Floor: -220~223 dBc/Hz
- Chip size: 1.44*1.74*0.18mm

Function Diagram



Electrical Specifications (Ta=+25℃)

Parameter		Condition	Min	Typ.	Max	Unit
RF Input		800MHz	-10	-	13	dBm
		6500MHz	-10	-	13	
Max. Pre-divide Output Frequency		P=8	-	-	350	MHz
		P=16	-	-	375	
PFD Max. Phase Frequency		-	-	-	100	MHz
Charge Pump Current		SPEC	0.65	-	5.2	mA
RSET Range		SPEC	3	-	11	KΩ
Supply	AVDD	-	3.2	3.3	3.6	V
	DVDD	-	AVDD			
	VP	-	3.2	-	5.5	
	AIDD+DIDD	-	-	19	-	mA
	IP	-	-	1	-	
Phase Noise	Phase noise @6.5GHz output	@10KHz offset and 5MHz PFD Freq.	-	-96	-	dBc/Hz
	Spurious @6.5GHz output	@5MHz offset and 100MHz PFD Freq.	-	-70	-	dBc

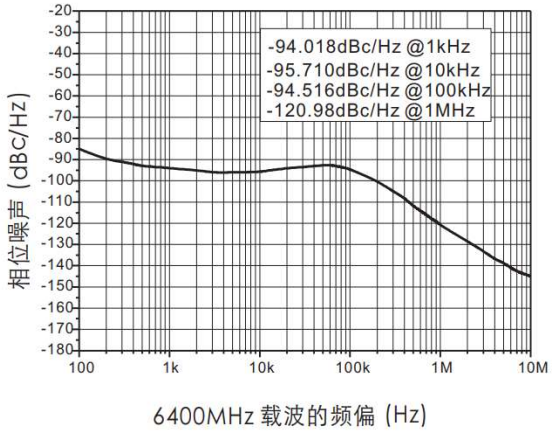
rREF=100MHz, fPFD=5MHz, fRF=6500MHz, N=1300, loopB/W=100KHz, VCO=HEM716 6.3~6.8GHz

Absolute Max Ratings

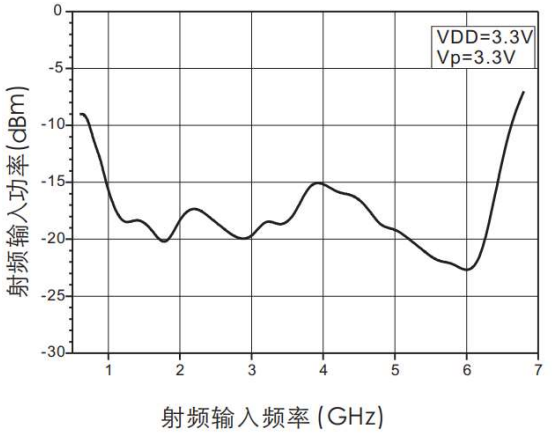
Vp	+3.6Vdc	Operating Temperature	-55 ~ +125℃
Junction Temperature	175℃	ESD (HBM)	Class 1A
Storage Temperature	-65 ~ +150℃	ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS	

Test Curves

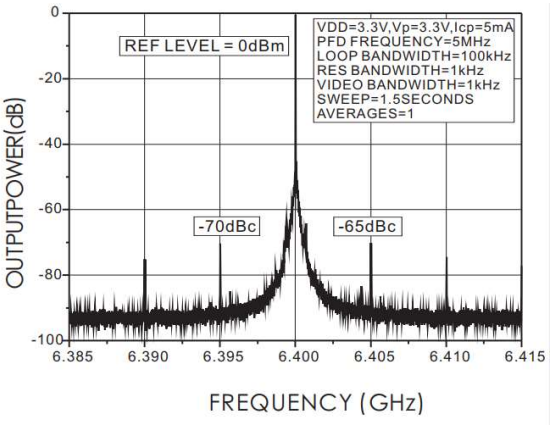
Phase Noise (6.4GHz, 4MHz and 100KHz), T=+25℃



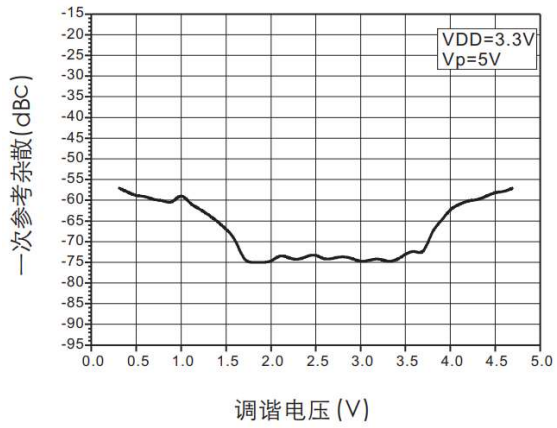
RF Input Sensitivity



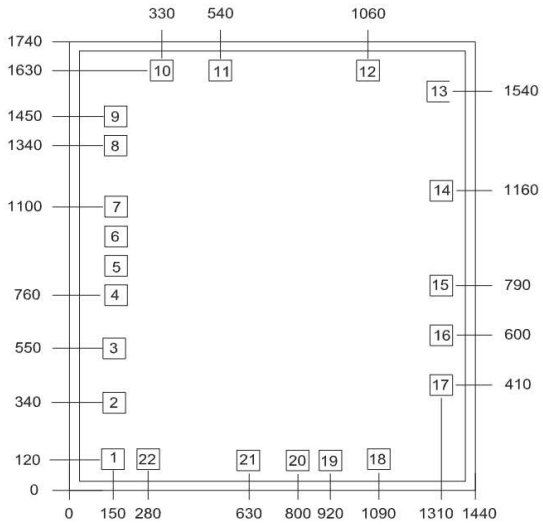
Spurious (6.4GHz, 5MHz and 100KHz)



Spurious (6.4GHz, 5MHz and 100KHz)



Outline Size



Note:

1. Unit: um
2. Bonding pads is AL plated, size: 80*90um

Pads Definition

Pad	Symbol	Description
1	AVDD	Analog power supply, range 3.0V~3.6V, Decoupled capacitor to Analog GND should be close to this pad, AVDD value must be equal to DVDD.
22		
2	RFINA	RF pre-divide A input, connect to output ac coupling of VCO as small signal input of this pad.
3	RFNAB	RF pre-divide B input, please apply small block capacitor for ground, typical value is 100pF.
4	A GND	Analog ground, this is ground loop pad of AVDD.
5		
6		
7		
8	CP GND	Charge pump ground, this is ground loop pad of charge pump
9		
10	CP	Charge pump output, this pad provides ICP current to external loop filter, to tune external VCO.
11	RSET	Connect this pad and GND by a resistor, set charge pump max output current, voltage of this pad is 0.66V, relation of ICP MAX and RSET: ICP MAX=26.5/RSET. When RSET=5.1kΩ, ICP MAX=5.2mA.
12	VP	Charge pump supply, this pad has to be equal or bigger than AVDD. When AVDD is 3.3V, VP max can be 5V.
13	DVDD	Digital supply, voltage of this pad should be equal to AVDD, decoupling capacitor should be close to this pad as much as possible.
14	MUXOUT	MUX output, can examine and lock indicator, RF signal divided and Reference input etc from outside.
15	LE	Load, CMOS input, when LE is high level, data in shift register load into latch which is chosen by 4 LSB control bits.
16	DATA	Series data input, series data is loaded in MSB priority mode, 2 LSB is as control bit. This input is high impedance CMOS input.
17	CLK	Series clock input, at CLK rising edge the data input 24 bits shift register separately. This input is high impedance CMOS input.
18	CE	Logic low enablement component is turn off state charge pump output is at three states. Logic high enablement component start working, state is decided by F2 of power down.
19	DGND	Digital ground, this is ground loop pad of DVDD.
20		
21	REFIN	Reference input, this is CMOS input, nominal threshold is VDD/2, has 100KΩ DC equivalent input resistor, this input can be driven by TTL or CMOS oscillator, or DC coupling.