

Performance

- Technology: 0.35um Power HEMT
- Frequency: 3.0~3.4GHz
- Typical Pout : 80W
- Typical Gain: 12dB
- Typical PAE: 60%
- Bias: 28V/-3V
- Package: Metal Ceramic

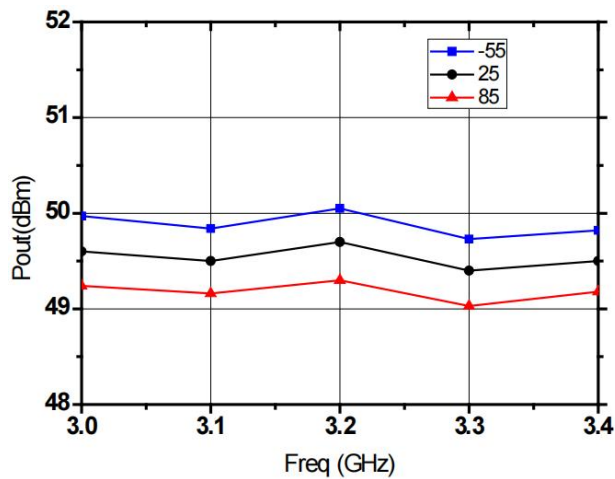


Electrical Specifications (TA=25°C, Vd=28V, Vg=-3V, t=200us, D=20%, F: 3.0~3.4GHz)

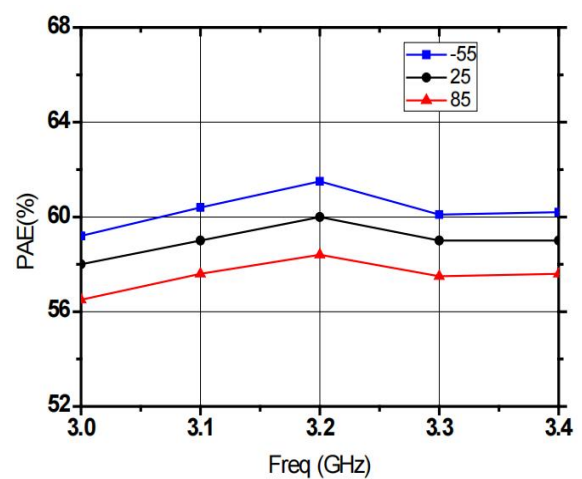
Symbol	Parameter	Min	Typical	Max	Unit
Pout	Output Power	-	80	-	W
Gp	Power Gain	-	12	-	dB
η_{add}	Power Added Efficiency	-	60	-	%
ΔGp	Gain Flatness	-0.5	-	+0.5	dB
Rth	Thermal Resistance	-	-	0.4	°C/W

Test Curves

Pout&Freq. @ Different Temp.



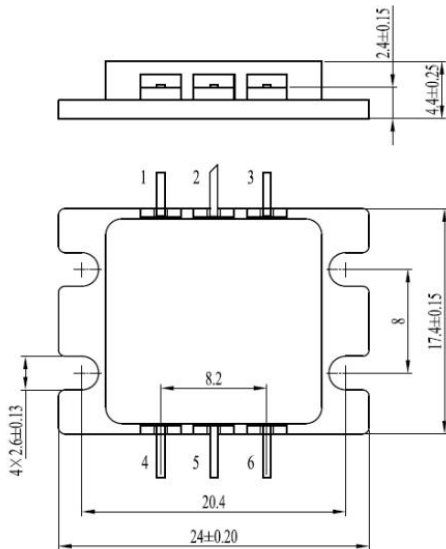
PAE&Freq. @ Different Temp.



Absolute Max Ratings (TA=25°C)

Symbol	Parameter	Value	Remark
Vd	Drain Voltage	80V	
Vg	Grid Voltage	-5V	
Pd	DC Dissipation	250W	25°C
Tch	Channel Temperature	175°C	【1】
Tm	Mounting Temperature	300°C	1 min, N2 Protection
Tstg	Storage Temperature	-55~175°C	

【1】 Exceeding any one or combination of these limits may cause permanent damage.

Outline Drawing	Dimension Symbol												
 The drawing shows a top view and a side view of the transistor. The top view is a square package with dimensions 24±0.20 mm by 17.4±0.15 mm. It has six pins: pins 1 and 3 are on the top, pin 2 is on the right, and pins 4, 5, and 6 are on the bottom. The distance between pins 1 and 3 is 8.2 mm. The distance between pins 4, 5, and 6 is 20.4 mm. The side view shows a height of 4.4±0.25 mm and a top thickness of 2.4±0.15 mm. There are also dimensions for the mounting tabs: 4×2.6±0.13 mm and 8 mm.	<table><tr><th>No</th><th>Function</th><th>No</th><th>Function</th></tr><tr><td>1、3</td><td>Vg</td><td>4、6</td><td>Vd</td></tr><tr><td>2</td><td>RFin</td><td>5</td><td>RFout</td></tr></table>	No	Function	No	Function	1、3	Vg	4、6	Vd	2	RFin	5	RFout
No	Function	No	Function										
1、3	Vg	4、6	Vd										
2	RFin	5	RFout										

Application Circuit

The diagram shows a GaN Transistor in a central package with pins labeled VG, IN, OUT, and VD. The circuit includes the following components and connections:

- Gate (VG) Biasing:** A DC bias voltage V_{GS} is applied through a series of capacitors C3, C2, and C1. A 500Ω resistor (C7) is connected between the input and the gate.
- Drain (VD) Load:** A DC drain voltage V_{DS} is applied through a series of capacitors C6, C5, and C4. A 500Ω load resistor (C8) is connected between the drain and the output.
- Input/Output:** The input signal is applied to the IN pin, and the output signal is taken from the OUT pin.

Symbol	Value
C1	100pF
C2	1000pF
C3	47uF
C4	100pF
C5	1000pF
C6	10uF
C7	20pF
C8	20pF

Note:

- (1) The typical packaging form is C164-2 shell packaging;
- (2) Connect the circuit according to the diagram, pay attention to anti-static, and ensure good grounding and heat dissipation when using power devices;
- (3) In order to ensure the good performance of the power module, the capacity value of power filter and energy storage capacitor shall be reasonably selected according to the modulation mode during pulse operation