

Performance

- Technology: 0.35um Power HEMT
- Frequency: 3.1~3.3GHz
- Typical Pout : 170W
- Typical Gain: 12dB
- Typical PAE: 60%
- Bias: 32V/-3V
- Package: Metal Ceramic

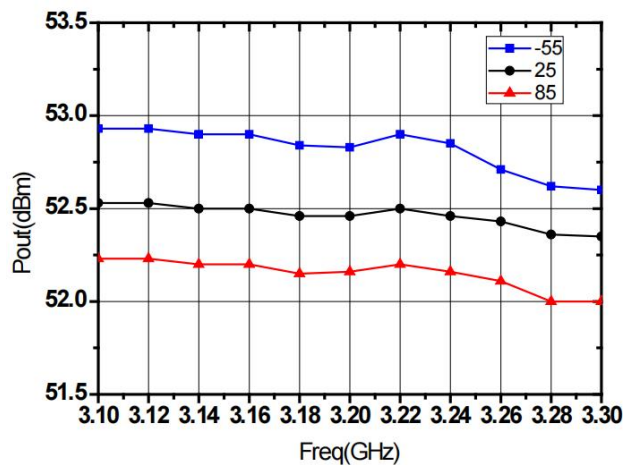


Electrical Specifications ($T_A=25^{\circ}\text{C}$, $V_d=32\text{V}$, $I_d=0.1\text{A}$, $PL=60\mu\text{s}$, $D.C=15\%$, $F: 3.1\sim 3.3\text{GHz}$)

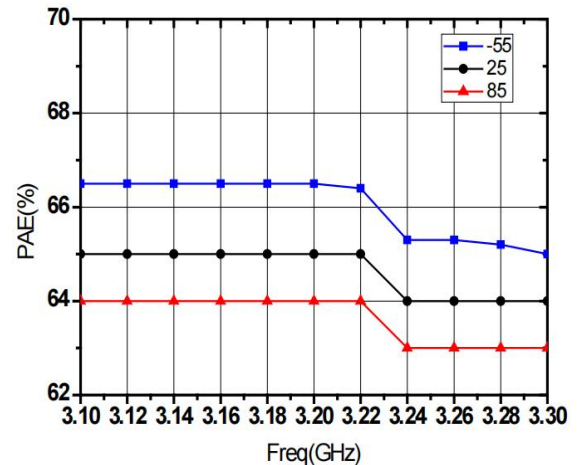
Symbol	Parameter	Min	Typical	Max	Unit
Pout	Output Power	-	170	-	W
Gp	Power Gain	-	12	-	dB
η_{add}	Power Added Efficiency	-	60	-	%
ΔG_p	Gain Flatness	-0.2	-	+0.2	dB
Rth	Thermal Resistance	-	-	0.24	$^{\circ}\text{C}/\text{W}$

Test Curves

Pout&Freq. @ Different Temp.



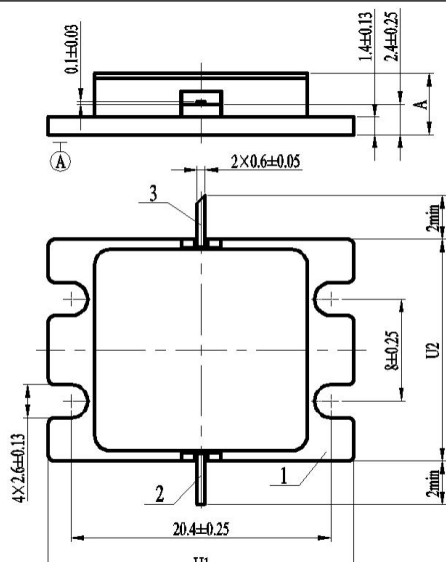
PAE&Freq. @ Different Temp.



Absolute Max Ratings (T_A=25°C)

Symbol	Parameter	Value	Remark
V _d	Drain Voltage	80V	
V _g	Grid Voltage	-5V	
P _d	DC Dissipation	120W	25°C
T _{ch}	Channel Temperature	225°C	【1】
T _m	Mounting Temperature	300°C	1 min, N ₂ Protection
T _{stg}	Storage Temperature	-55~150°C	

【1】 Exceeding any one or combination of these limits may cause permanent damage.

Outline Drawing	Dimension Symbol														
 The drawing shows a top view and a side view of the transistor package. The top view is a square with rounded corners, with dimensions U1 (width), U2 (height), and 20.4±0.25 (width of the central square). The side view shows the package height A, with dimensions 0.1±0.05, 1.4±0.13, and 2.4±0.25. The package is mounted on a substrate with dimensions 2X0.6±0.05 and 3. The package is labeled with 1, 2, and 3.	<table><tr><th rowspan="2">Symbol</th><th colspan="2">Value (unit: mm)</th></tr><tr><th>Min.</th><th>Max.</th></tr><tr><td>U1</td><td>23.80</td><td>24.20</td></tr><tr><td>U2</td><td>17.20</td><td>17.60</td></tr><tr><td>A</td><td>-</td><td>5.2</td></tr></table>	Symbol	Value (unit: mm)		Min.	Max.	U1	23.80	24.20	U2	17.20	17.60	A	-	5.2
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	Min.	Max.													
U1	23.80	24.20													
U2	17.20	17.60													
A	-	5.2													

Application Circuit

The image displays two circuit diagrams for a GaN transistor. The left diagram shows a common-source configuration with a microstrip line TL1 ($\lambda/4$) at the gate, a resistor R1 (15 Ω) in series with the gate, and a microstrip line TL2 ($\lambda/4$) at the drain. The right diagram shows a similar configuration but with a resistor R2 (50 Ω) in series with the gate and a microstrip line TL2 ($\lambda/4$) at the drain. Both diagrams include a DC voltage source VDC and various capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9) for filtering and isolation.

Parameter	Symbol	Value	Unit
Filter capacitor	C1,C2,C4, C5,C6	1000	pF
Filter capacitor	C3,C7	100	pF
DC isolation capacitance	C8,C9	10	pF
Stabilizing resistance	R1	15	Ω
Resistance	R2	50	Ω
Microstrip line	TL1,TL2	$\lambda/4$	-

Note:

- (1) This product is an internal matching tube, with input and output impedance values of 50 ohms;
- (2) The power-on sequence shall be in strict accordance with the sequence of applying negative power first and then positive power. When power-off, the leakage voltage shall be reduced first and then the grid voltage shall be reduced;
- (3) This product is a high-power device. Pay attention to heat dissipation during use. The higher the shell temperature is, the shorter the service life is. The service temperature should not be higher than 80 °C;
- (4) This product is an electrostatic sensitive device. It needs to pay attention to electrostatic protection during storage and use, and it needs to be grounded well during use.