

Performance

- Technology: 0.25um Power GaN HEMT
- Frequency: 7.7~8.5GHz
- Typical Pout : 48dBm(CW)
- Typical Gain: 8dB
- Typical PAE: 45%
- Bias: 28V/-2~-3V
- Package: Metal Ceramic

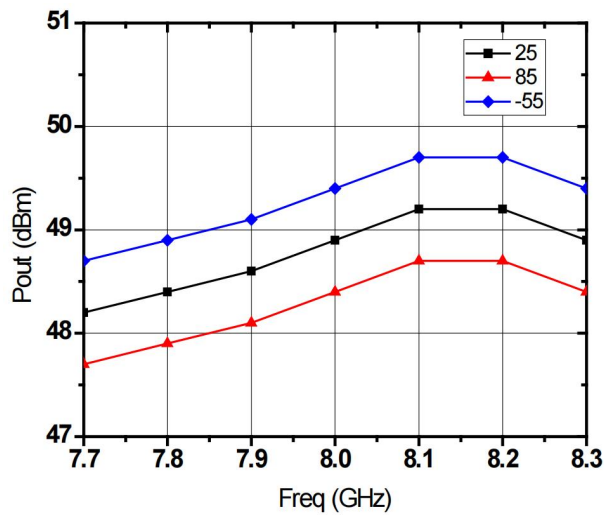


Electrical Specifications (TA=25°C, Vd=28V, Vg= -2~-3V, Id≈8A, F: 7.7~8.5GHz)

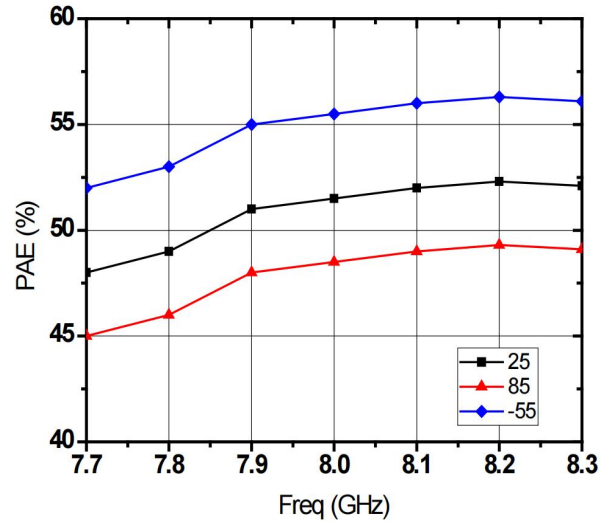
Symbol	Parameter	Min	Typical	Max	Unit
Pout	Output Power	-	48	-	dBm
Gp	Power Gain	-	8	-	dB
η_{add}	Power Added Efficiency	-	45	-	%
Rth	Thermal Resistance	-	-	-	°C/W
ΔGp	Gain Flatness	-0.8	-	+0.8	dB

Test Curves

Pout&Freq. @ Different Temp.



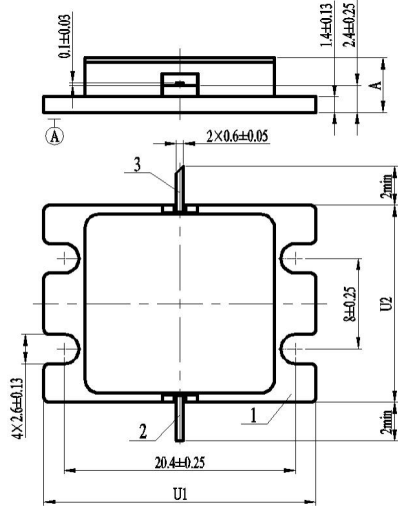
PAE&Freq. @ Different Temp.

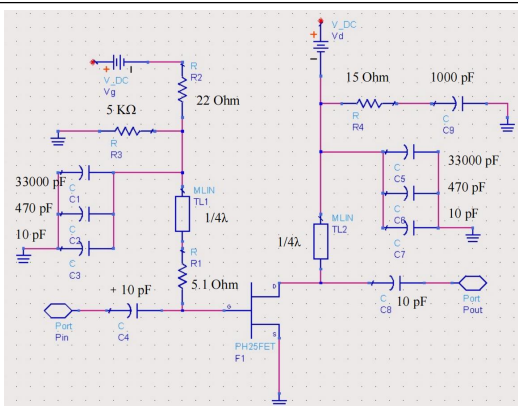


Absolute Max Ratings (T_A=25°C)

Symbol	Parameter	Value	Remark
V _d	Drain Voltage	40V	
V _g	Grid Voltage	-5V	
P _d	DC Dissipation	100W	25°C
T _{ch}	Channel Temperature	225°C	【1】
T _m	Mounting Temperature	300°C	1 min, N ₂ Protection
T _{stg}	Storage Temperature	-55~175°C	

【1】 Exceeding any one or combination of these limits may cause permanent damage.

Outline Drawing	Dimension Symbols														
 The drawing shows a top view and a side view of the transistor. The top view is a square with rounded corners, with dimensions U1 (width) and U2 (height). The side view shows the thickness of the device, with dimensions A (total thickness) and 2mm (mounting pad thickness). Other dimensions include 20.4±0.25, 8±0.25, 4±0.13, 2×0.6±0.05, 1.4±0.13, 2.4±0.25, and 0.1±0.05.	<table><tr><th rowspan="2">Symbol</th><th colspan="2">Value (unit: mm)</th></tr><tr><th>Min.</th><th>Max.</th></tr><tr><td>U1</td><td>23.80</td><td>24.20</td></tr><tr><td>U2</td><td>17.20</td><td>17.60</td></tr><tr><td>A</td><td>-</td><td>5.2</td></tr></table>	Symbol	Value (unit: mm)		Min.	Max.	U1	23.80	24.20	U2	17.20	17.60	A	-	5.2
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U1	23.80	24.20													
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Application Circuit	Pad Definition								
 The application circuit diagram shows a GaN transistor (PH25FET F1) connected to a source (Pin) and a drain (Pout). The gate is connected to a biasing network consisting of a 5 KΩ resistor (R3) and a 22 Ohm resistor (R2). The source is connected to a 5.1 Ohm resistor (R1) and a 10 pF capacitor (C4). The drain is connected to a 15 Ohm resistor (R4) and a 1000 pF capacitor (C8). The gate is also connected to a 33000 pF capacitor (C1) and a 470 pF capacitor (C3). The drain is connected to a 33000 pF capacitor (C5) and a 470 pF capacitor (C7). The gate is connected to a 1/4λ transmission line (TL1) and the drain is connected to a 1/4λ transmission line (TL2).	<table> <tr> <th>No</th><th>Function</th></tr> <tr> <td>1</td><td>Source</td></tr> <tr> <td>2</td><td>V_d</td></tr> <tr> <td>3</td><td>V_g</td></tr> </table>	No	Function	1	Source	2	V _d	3	V _g
No	Function								
1	Source								
2	V _d								
3	V _g								

Note:

- (1) The device is an internal matching device, and the input and output impedance values are both 50 ohms;
- (2) Power-on sequence: first add negative electricity to the gate, and then add positive electricity to the drain.