

### Feature

Pass Bands: 0.8GHz~1.4GHz, 1.2GHz~2.2GHz, 2GHz~3.5GHz, 3GHz~5GHz, 4.5GHz~7.5GHz, 7GHz~11.5GHz, 11~18GHz Insertion Loss in pass bands: ≤8dB Size: 4.5x5x0.1mm

# Description

This device is a GaAs monolithic integrated FET switch filter bank chip. Adopt +5V/0V logic control, and switching speed is less than 30ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

Numbering Rules	Absolute Rating	
BW SBFX - XXX/XXX - XCX 1 2 3 4 5 6 7 1. Series BW	Input Power	27dBm
<ol> <li>SBF means switch BPF bank</li> <li>Channel numbers</li> </ol>	Storage Temperature	-65~+150°C
<ol> <li>4. Starting frequency (GHz)</li> <li>5. Cut-off frequency (GHz)</li> <li>6. Section numbers.</li> <li>7. Insertion loss at F0 (dB)</li> </ol>	Operating Temperature	-55~+125℃

# Electrical Specifications 1 (T<sub>A</sub>=+25°C)

Spec.	Pass band 1	Pass band 2	Pass band 3	Pass band 4	Unit
Freq. Range	0.8~1.4	1.2~2.2	2~3.5	3~5	GHz
Insertion Loss	≤8.0	≤8.0	≤8.0	≤8.0	dB
Ripple in BW	≤1.5	≤1.5	≤1.5	≤1.5	dB
Rejection	≥30@0.4&2GHz	≥30@0.7&3.4GHz	≥30@1.3&4.2GHz	≥30@2.1GHz ≥30@6.3GHz	dBc
VSWR	≤2				

# Electrical Specifications 2 (T<sub>A</sub>=+25°C)

Spec.	Pass band 5	Pass band 6	Pass band 7	Unit
Freq. Range	4.5~7.5	7~11.5	11~18	GHz
Insertion Loss	≤8.0	≤8.0	≤8.0	dB
Ripple in BW	≤1.5	≤1.5	≤1.5	dB
Rejection	≥30@3.4GHz ≥30@8.9GHz	≥30@5.5GHz ≥30@13.8GHz	≥30@8.8GHz ≥30@21.5GHz	dBc
VSWR		≤2		-

S2P file name: BWSBF7-R8\_18-7C7.s2p



#### **Typical Test Curves**

Pass band 1 Insertion Loss VS Frequency (TA=25°C)



Pass band 3 Insertion Loss VS Frequency (TA=25°C)











Pass band 4 Insertion Loss VS Frequency (TA=25°C)







Seven-band amplitude-frequency characteristics









**Mechanical Specification** 

IN

0.9 - 11V3 0.7 - 12V2 0.5 - 13V1 0.3 - 13VEE V1 V2 V3 VEE V1 02 V3 0 - 1 1 1 1

0.3 - 0.5 - 0.7 - 0.9 - 0

0--0



IN / OUT Port



Contro	Control Voltage (VEE=-5V)		Dass bands (CHz)
V1	V2	V3	
0	0	0	0.8~1.4
0	5	0	1.2~2.2
0	0	5	2~3.5
0	5	5	3~5
5	0	5	4.5~7.5
5	0	0	7~11.5
5	5	5	11~18

2 OUT

4.5 -



#### **PINS Definitions**

NO	Symbol	Description
1,2	IN, OUT	RF input, RF output (interchangeable)
6,7,14,15	VEE	Driver supply voltage (select one)
5,8,13,16	V1	Control port (select one)
4,9,12,17	V2	Control port (select one)
3,10,11,18	V3	Control port (select one)

#### Notes:

- 1. Dimensions are um. Tolerance: ±0.05mm
- 2. Die thickness is 0.1mm
- 3. Typical bond pad is 100um  $\star 100 \text{um}$  , which is 50um away from chip edge.
- 4. The bottom of the device is gold plated, should be grounded.
- 5. Cannot bond on through-holes

#### **Recommended Assembly Diagrams**

#### **Functional Diagram**



## **Application Notes:**

1) Use in a clean environment. Be careful not to touch the chip surface.

2) It is recommended to use two 25um diameter gold wires for bonding. The length of the bonding wire should be less than 400um.

3) Use 80/20 gold-tin sintering. The sintering temperature should not exceed 300 °C. The sintering time should be as short as possible and should not exceed 30 seconds.

- 4) This product is an electrostatic sensitive device. Pay attention to anti-static during storage and use.
- 5) Store in a dry, nitrogen environment.
- 6) Do not try to clean the chip surface with dry or wet chemical methods.
- 7) Please contact the supplier if you have any questions.